

DECLARATION

As the below named sole inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name; that I believe I am the first and original of the invention entitled:

PLANAR TRANSISTOR STRUCTURE USING ISOLATION IMPLANTS FOR IMPROVED V_{ss} RESISTANCE AND FOR PROCESS SIMPLIFICATION

described and claimed in the specification which is attached hereto that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above; that I do not know and do not believe the same was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application, that I acknowledge my duty to disclose information of which I am aware that is material to the examination of this application as defined by 37 C.F.R. §1.56, and that no application for patent or inventor's certificate on said invention has been filed in any country foreign to the United States of America by my or by my legal representatives or assigns.

Address all telephone calls to Mr. Sawyer at telephone number (650) 493-4540 and all correspondence

**Joseph A. Sawyer Jr.
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

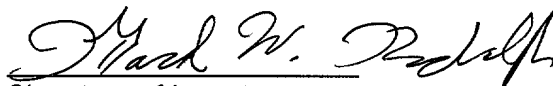
Name of **first/sole** Inventor: **Mark RANDOLPH**

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Post Office Address: **Same as above**

Country of Citizenship: **United States of America**

12/14/01
Date


Signature of Inventor

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: **Mark RANDOLPH**

Title: **PLANAR TRANSISTOR STRUCTURE USING ISOLATION IMPLANTS FOR
IMPROVED V_{ss} RESISTANCE AND FOR PROCESS SIMPLIFICATION**

**POWER OF ATTORNEY BY ASSIGNEE
AND EXCLUSION OF INVENTOR UNDER 37 C.F.R. SEC. 1.32**

Assistant Commissioner of Patents
Box Patent Applications
Washington, D.C. 20231

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T.C. 4304

ADVANCED MICRO DEVICES, Inc., a Delaware Corporation, having become the owner of all rights in and to the above-identified application by virtue of an Assignment executed by the inventor concurrently with the execution of the application, said Assignment being submitted herewith for recording, hereby appoints:

Elizabeth A. Apperley Reg. No. 36,428
Bradley Botsch, Reg. No. 34,552
Michael Caywood, Reg. No. 37,797
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as their attorneys, to prosecute said application and to transact in connection therewith all business in the Patent and Trademark Office and before competent International Authorities; said appointment to be to the exclusion of the inventor and his attorneys in accordance with the provisions of 37 C.F.R. 1.32.

Date: December 14, 2001


Name: RICHARD J. RODDY

Title: CHIEF PATENT AND TRADEMARK COUNSEL
AND ASSISTANT SECRETARY